7/ Reconsideration
9/11/03

I hereby certify that this correspondence is being sent by facsimile transmission to: Examiner – Allen E. Quillen at Fax No.: 1-703-746-7194

On August 20, 2003

TOWNSEND and TOWNSEND and CREW LLP

By: J. Matthew Zigmant

PATENT
Attorney Docket No.: 019680-000200US

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Allen E. Quillen
Alexander L. Minkin	Art Unit: 2676
Application No.: 09/712,632	COMMUNICATION REGARDING RESPONSE TO OFFICE ACTION FILED ON JUNE 12, 2003
Filed: November 13, 2000	
For: CIRCUIT AND METHOD FOR ADDRESSING A TEXTURE CACHE	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication is in regards to a phone conversation held August 20, 2003, between Examiner Allen E. Quillen and applicant's representative J. Matthew Zigmant, registration number 44,005. The Applicant and his representative would like to thank Examiner Quillen for his time and consideration of these matters.

Claim 10 requires "forming an index signal by concatenating middle order bits of the s coordinate, middle level bits of the t coordinate, and at least one bit of the level of detail." The cited reference Van Hook (et al.) (6,353,438) does not appear to provide this. The cited reference does show the level of detail used as part of a tag in Figure 12. Also, the abstract states that "the level of detail may be specified as part of the tag information."

But a tag is not the same as an index. These are different address portions and are used for different tasks by a cache system. For example, the first attached page is a block diagram that can be found on the internet at http://www.cs.tcd.ie/Michael.Brady/ISD/MSc%20System%20Design%205.ppt

As the data RAM (cache) is loaded with data, tags corresponding to the data are stored in the Tag RAM. (This is analogous to a list of people in a movie theater as discussed in today's phone conversation.) The index is decoded and used to identify which block in cache the data is to be written to. (This is analogous to an usher seating people in the movie theater.)

When data is read, the index is decoded in order to select a location in the Tag RAM. The tag at that location in the Tag RAM is compared to the tag of the present address. If there is a match (cache hit) then the index identifies the location of the data in the cache, and the data is read.

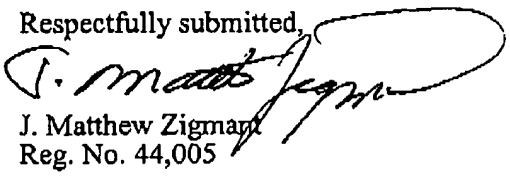
This is summarized on the last attached page, found at web site http://www-inst.eecs.berkeley.edu/~cs61c/lectures/apr23slides.pdf

As is shown, the index is used to select a block in cache, while the tag is used to check if the correct block is in cache (whether there is a cache hit.) As is shown consistently in Figures 11 and 12 of Van Hook, Figure 3 of the present application, and the attached two pages, the index and tag are different portions of an address and are used for different functions.

Also, claims 11-13 require the index signal to have "at least one bit of texture identification," "at least one bit of the r coordinate," and "at least one bit of the main memory address." Van Hook does not appear to use these as part of either a tag or index.

Thank you again. The undersigned can be reached at 650-752-2456, or by e-mail at jmzigmant@townsend.com.

Respectfully submitted,



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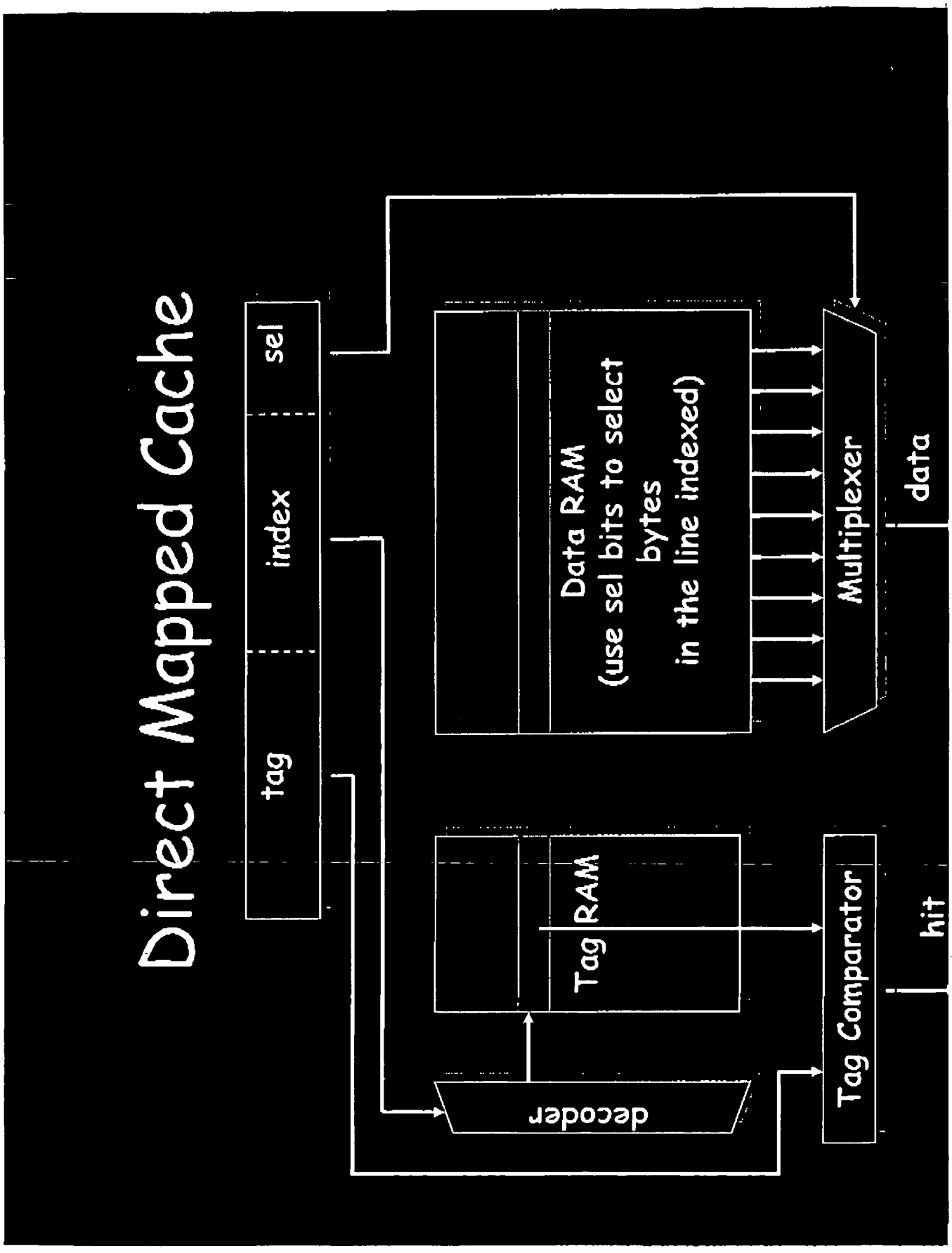
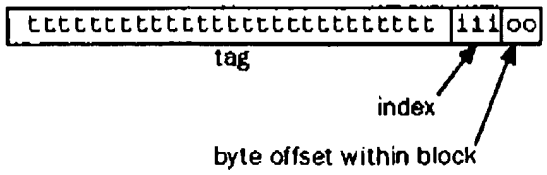


Accessing elements of a direct-mapped cache

- Divide memory reference into three fields:
  - *byte offset* within block;
  - index to select the block;
  - tag to check if we have the correct block.



- One part of a cache entry is the tag; another part is the contents of memory at the given address; a third is a "valid" bit.